In the Claims:

1-5. (Cancelled)

6. (Currently Amended) A method of manufacturing a semiconductor device, comprising:

forming an oxide film ~~and a first silicon layer~~ on a semiconductor substrate comprising a surface portion of a first conductivity type;

forming a first silicon layer on the oxide film;

selectively forming an oxidation resistance film on the first silicon layer;

forming a field oxide film by thermal oxidation in an area of the semiconductor substrate not covered by the oxidation resistance film;

removing the oxidation resistance film;

forming a resistance layer of a second conductivity type [[on]] in the surface portion of the semiconductor substrate by ion implantation of an impurity of the second conductivity type piercing ~~through~~ the first silicon layer and the oxide film;

forming a second silicon layer covering the ~~whole area of the device~~ the first silicon layer and the field oxide film;

forming a resistance bias electrode layer [[on]] above the resistance layer ~~through a~~ by patterning [[of]] the first and second silicon layers; and

forming a wiring layer for providing the resistance bias electrode layer with a predetermined voltage.

7. (Currently Amended) The method of manufacturing the semiconductor device of claim 6, wherein ~~both of~~ the first and second silicon layers are made of polysilicon or amorphous silicon.

8. (Original) The method of manufacturing the semiconductor device of claim 6 or 7, wherein the oxidation resistance film is a silicon nitride film.

9. (Currently Amended) The method of manufacturing the semiconductor device of claim 6, wherein the wiring layer contacts with the resistance layer at [[the]] a middle portion of the resistance layer [[in]] with respect to its lateral direction.

10. (Currently Amended) A method of manufacturing a semiconductor device having a MOS transistor and a resistor element on a semiconductor substrate, comprising:

forming an oxide film ~~and a first silicon layer~~ on a semiconductor substrate comprising a surface portion of a first conductivity type;

forming a first silicon layer on the oxide film;

selectively forming an oxidation resistance film on the first silicon layer over ~~both of~~ a MOS transistor forming region and a resistance forming region of the semiconductor substrate;

forming a field oxide film by thermal oxidation in an area of the semiconductor substrate not covered by the oxidation resistance film;

removing the oxidation resistance film;

forming a resistance layer of a second conductivity type [[on]] in the surface portion of the semiconductor substrate by ion implantation of an impurity of the second conductivity type piercing ~~through~~ the first silicon layer and the oxide film [[on]] in the resistance forming region;

forming a second silicon layer covering the ~~whole area of the device~~ MOS transistor forming region and the resistance forming region;

forming simultaneously a resistance bias electrode layer [[on]] above the resistance layer ~~through the~~ and a gate electrode of the MOS transistor in the MOS transistor forming region by patterning [[of]] the first and second silicon layers ~~and simultaneously forming the gate electrode of the MOS transistor~~;

forming simultaneously a source layer and a drain layer of the MOS transistor and a pair of electrode pad layers of the resistance layer; and

forming a wiring layer for providing the resistance bias electrode layer with a predetermined voltage.

11. (Currently Amended) The method of manufacturing the semiconductor device of claim 10, wherein the first and second silicon layers are made of polysilicon or amorphous silicon.

12. (Currently Amended) The method of manufacturing the semiconductor device of claim 10 or 11, wherein the oxidation resistance film is a silicon nitride film.

13. (Currently Amended) The method of manufacturing the semiconductor device of claim 10, wherein the wiring layer contacts with the resistance layer at [[the]] a middle portion of the resistance layer [[in]] with respect to its lateral direction.